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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/936,032	03/11/2002	Michael Nicolaidis	514842000100	9437

7590 05/02/2005

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EXAMINER	
GANDHI, DIPAKKUMAR B	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 05/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/936,032	NICOLAIDIS, MICHAEL	
	Examiner	Art Unit	
	Dipakkumar Gandhi	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

1. Applicant's request for reconsideration filed on 1/4/2005 has been reviewed.

2. The amendment filed on 1/4/2005 has been entered, including amended specification and amended claims.

3. The foreign priority claim filed on 3/11/2002 is entered after reviewing the documents previously filed.

4. Applicant's arguments with respect to claims 1-10 have been considered but are moot in view of the new ground(s) of rejection.

Specification

5. The abstract of the disclosure is objected to because the abstract sheet also mentions amendments to the specification. An abstract on a separate sheet is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

7. Claim 8 is rejected under 35 U.S.C. 102(a) as being anticipated by Kanekawa et al. (US 5,802,266)

Kanekawa et al. anticipate claim 8.

Kanekawa et al. teach a combinatory logic circuit (10) having at least one output (A) connected to a first synchronization flip-flop (70) rated by a clock (CK), a second flip-flop (71) rated by the clock and receiving said output delayed by a predetermined duration (8), and a circuit (74) for analyzing the flip-flop outputs, the analysis circuit indicating an error if the flip-flop outputs are different (fig. 49, abstract, col. 27, line 58-col. 28, line 4, col. 28, lines 8-12, Kanekawa et al.).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. Claims 1, 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Helm et al. (US 5,072,450) in view of Byers et al. (US 5,416,362).

As per claim 1, Helm et al. teach a circuit protected against transient disturbances, comprising a combinatory logic circuit (10) having at least one output (A), a circuit (20, 11) for generating an error control code for said output (figure 1, col. 3, lines 20-33, Helm et al.).

However Helm et al. do not explicitly teach the specific use of a memory element (24, 24') arranged at said output, controlled by the control code generation circuit to be transparent when the control code is correct, and to keep its state when the control code is incorrect.

Byers et al. in an analogous art teach that the present invention ... latched through the system (col. 1, line 64-col. 2, line 2, Byers et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Helm et al.'s patent with the teachings of Byers et al. by including an additional step of using a memory element (24, 24') arranged at said output, controlled by the control code generation

circuit to be transparent when the control code is correct, and to keep its state when the control code is incorrect.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to transmit the output of a circuit only when the output is error free.

- As per claim 2, Helm et al. and Byers et al. teach the additional limitations.

Helm et al. teach the protected circuit, wherein the error control code generation circuit includes a circuit (20) for calculating a parity bit (P) for said output (A) and a circuit (22) for checking the parity of the output and of the parity bit (figure 1, col. 3, lines 20-33, Helm et al.).

11. Claims 3, 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Helm et al. (US 5,072,450) and Byers et al. (US 5,416,362) as applied to claim 1 above, and further in view of Stewart et al. (US 4,464,754).

As per claim 3, Helm et al. and Byers et al. substantially teach the claimed invention described in claim 1 (as rejected above). Byers et al. also teach that the memory element (24') being provided to be transparent in certain conditions and to keep its state in different conditions (col. 1, line 64-col. 2, line 2, Byers et al.).

However Helm et al. and Byers et al. do not explicitly teach the specific use of the error control code generation circuit including a duplicated logic circuit (11) and the outputs of the logic circuit (10) and of the duplicated circuit (11) are identical in certain conditions and the outputs are different in other conditions.

Stewart et al. in an analogous art teach that the memory system of FIG. 1 ...other chips of a set (col. 1, line 61-col. 2, line 10, Stewart et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Helm et al.'s patent with the teachings of Stewart et al. by including an additional step of using the error control code generation circuit including a duplicated logic circuit (11) and the outputs of the logic circuit (10) and of the duplicated circuit (11) are identical in certain conditions and the outputs are different in other conditions.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to determine if there is an error in the output of the circuit and send the output to other circuits only when the output has no error.

- As per claim 5, Helm et al., Byers et al. and Stewart et al. teach the additional limitations.

Stewart et al. teach that the memory element (24') is formed from a logic gate providing the output of the logic circuit, this logic gate including at least two first transistors (MN1, MP2) controlled by a signal (a) of the logic circuit and at least two second transistors (MP1, MN2) controlled by the corresponding signal (a*) of the duplicated circuit, each of the second transistors being connected in series with a respective one of the first transistors (figure 2B, col. 5, lines 16-21, lines 45-55, Stewart et al.).

12. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Helm et al. (US 5,072,450) and Byers et al. (US 5,416,362) as applied to claim 1 above, and further in view of Paschal et al. (US 4,093,878).

As per claim 4, Helm et al. and Byers et al. substantially teach the claimed invention described in claim 1 (as rejected above). Byers et al. also teach that the memory element (24') being provided to be transparent in certain conditions and to keep its state in different conditions (col. 1, line 64-col. 2, line 2, Byers et al.).

However Helm et al. and Byers et al. do not explicitly teach the specific use of the error control code generation circuit including an element (90) for delaying the output by a predetermined duration greater than the maximum duration of transient errors and outputs of the logic circuit and of the delay element are identical in certain conditions and the outputs are different in other conditions.

Paschal et al. in an analogous arts teach that a delay element is inserted into the signal path of one of the passed signals. This, in turn, increases the time separation between the two signals (col. 2, lines 1-4, Paschal et al.). Paschal et al. also teach that the input logic gate changes state upon the coincidence of input signals (abstract, Paschal et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Helm et al.'s patent with the teachings of Paschal et al. by including an additional step of

using the error control code generation circuit including an element (90) for delaying the output by a predetermined duration greater than the maximum duration of transient errors and outputs of the logic circuit and of the delay element are identical in certain conditions and the outputs are different in other conditions.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to determine transient errors in the output of the circuit and send the circuit output when it is error free.

13. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Oprescu et al. (US 5,467,464) in view of Kanekawa et al. (US 5,802,266).

As per claim 6, Oprescu et al. teaches a combinatory logic circuit (10) having at least one output (A) connected to a first synchronization flip-flop (70,92) rated by a clock (CK), a second flip-flop (71, 93) connected to said output and rated by the clock delayed by a predetermined duration (8), and a circuit (74, 95) for analyzing the outputs of the flip-flops (fig. 5, col. 3, lines 51-66, Oprescu et al.).

However Oprescu et al. do not explicitly teach the specific use of the analysis circuit (95) indicating an error if the flip-flop outputs are different.

Kanekawa et al. in an analogous art teach that the logic circuit compares the output signals of the function blocks, and detects and error on the basis of the results of the comparison (abstract, Kanekawa et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Oprescu et al.'s patent with the teachings of Kanekawa et al. by including an additional step of using the analysis circuit (95) indicating an error if the flip-flop outputs are different.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the analysis circuit (95) indicating an error if the flip-flop outputs are different would provide the opportunity to determine an error in the circuit output.

14. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Oprescu et al. (US 5,467,464) and Kanekawa et al. (US 5,802,266) as applied to claim 6 above, and further in view of Ewen et al. (US 5,301,196).

As per claim 7, Oprescu et al. and Kanekawa et al. substantially teach the claimed invention described in claim 6 (as rejected above).

However Oprescu et al. and Kanekawa et al. do not explicitly teach the specific use of the protected circuit, wherein the second flip-flop (93) is controlled by the same clock as the first flip-flop, but by a different edge or level of this clock.

Ewen et al. in an analogous art teach that the outputs of these flip-flops, each triggered by a different edge of the clock, make up two demultiplexed data streams (abstract, Ewen et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Oprescu et al.'s patent with the teachings of Ewen et al. by including an additional step of using the protected circuit, characterized in that the second flip-flop (93) is controlled by the same clock as the first flip-flop, but by a different edge or level of this clock.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to delay the output of the second flip-flop circuit and provide two signal outputs from the two flip-flops that can be compared.

15. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over O'Lear (US 3,904,891) in view of Byers et al. (US 5,416,362) and Stewart et al. (US 4,464,754).

As per claim 9, O'Lear teaches a circuit protected against transient disturbances comprising: three identical logic circuits (10a, 11a, 10b), wherein each of the logic circuits is preceded by a two-input memory element (24a, 24b, 24c) respectively receiving the outputs of the two other logic circuits (figure 2, col. 5, lines 36-57, col. 7, lines 23-28, lines 33-39, O'Lear).

However O'Lear does not explicitly teach the specific use of each memory element being provided to be transparent in certain conditions and to keep its state in different conditions.

Byers et al. in an analogous art teach that the present invention ... latched through the system (col. 1, line 64-col. 2, line 2, Byers et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify O'Lear's patent with the teachings of Byers et al. by including an additional step of using each memory element being provided to be transparent in certain conditions and to keep its state in different conditions.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to transmit the output of a circuit only when the output is error free.

O'Lear also does not explicitly teach the specific use of two inputs (i.e. outputs from other circuits) are identical in certain conditions and the two inputs are different in other conditions.

Stewart et al. in an analogous art teach that the memory system of FIG. 1 ...other chips of a set (col. 1, line 61-col. 2, line 10, Stewart et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify O'Lear's patent with the teachings of Stewart et al. by including an additional step of using two inputs (i.e. outputs from other circuits) are identical in certain conditions and the two inputs are different in other conditions.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to determine if there is an error in the output of the circuit and send the output to other circuits only when the output has no error.

16. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over O'Lear (US 3,904,891), Byers et al. (US 5,416,362) and Stewart et al. (US 4,464,754) as applied to claim 9 above, and further in view of Lahey et al. (WO 97/40579).

As per claim 10, O'Lear, Byers et al. and Stewart et al. substantially teach the claimed invention described in claim 9 (as rejected above).

However O'Lear, Byers et al. and Stewart et al. do not explicitly teach specifically that the logic circuits are inverters and the memory elements include, in series, two P-channel MOS transistors and two N-channel MOS transistors, a first one of the inputs of the memory element being connected to the gates of a first one of the P-channel MOS transistors and of a first one of the N-channel MOS transistors, and the second input of the memory element being connected to the gates of the two other transistors.
Lahey et al. in an analogous art teach that Fig. 3 is a circuit for inverter ...the first inverter 42 (figure 3, page 6, lines 10-19, Lahey et al.).
Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify O'Lear's patent with the teachings of Lahey et al. by including additionally that the logic circuits are inverters and the memory elements include, in series, two P-channel MOS transistors and two N-channel MOS transistors, a first one of the inputs of the memory element being connected to the gates of a first one of the P-channel MOS transistors and of a first one of the N-channel MOS transistors, and the second input of the memory element being connected to the gates of the two other transistors.
This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to implement the logic functions using the inverters and store the data using the MOS transistors.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 571-272-3822. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dipakkumar Gandhi
Patent Examiner